

PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant : Troy A. Manning Attorney Docket No.: 500444.04  
Filed : Concurrently herewith  
Title : METHOD AND APPARATUS FOR GENERATING EXPECT DATA FROM A  
CAPTURED BIT PATTERN, AND MEMORY DEVICE USING SAME

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**INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

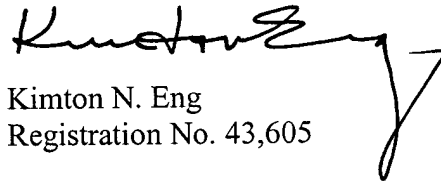
Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97 through 1.98, applicant wishes to make known to the Patent and Trademark Office the references set forth on the attached form PTO-1449. This application relies, under 35 U.S.C. § 120, on the earlier filing date of prior Application No. 10/268,351, filed October 9, 2002, which is a continuation of Application No. 09/924,139, filed August 7, 2001, issued November 5, 2002 as Patent No. 6,477,675 B2, which is a divisional of Application No. 09/146,860, filed September 3, 1998, issued February 19, 2002 as Patent No. 6,349,399 B1. The references listed on the attached Form PTO-1449 were submitted to and/or cited by the Patent and Trademark Office in these prior applications and, therefore, are not required to be provided in this application. If the Examiner wishes, copies will be provided upon request. Although the aforesaid references are made known to the Patent and Trademark Office in compliance with applicant's duty to disclose all information he is aware of which is believed relevant to the examination of the above-identified application, applicant believes that his invention is patentable.

Please acknowledge receipt of this Information Disclosure Statement and kindly make the cited references of record in the above-identified application.

Respectfully submitted,

DORSEY & WHITNEY LLP

A handwritten signature in black ink, appearing to read 'Kimton N. Eng', with a long, sweeping horizontal stroke extending to the right.

Kimton N. Eng  
Registration No. 43,605

KNE:asw

Enclosure:  
Form PTO-1449

1420 Fifth Avenue, Suite 3400  
Seattle, WA 98101  
Telephone (206) 903-8800  
Facsimile (206) 903-8820

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FORM PTO-1449  
(REV.7-80)U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.  
500444.04APPLICATION NO.  
Not Yet Assigned**INFORMATION DISCLOSURE STATEMENT***(Use several sheets if necessary)*APPLICANTS  
Troy A. ManningFILING DATE  
Concurrently herewithGROUP ART UNIT  
Not Yet Assigned**U.S. PATENT DOCUMENTS**

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	3,633,174	01/04/72	Griffin	340	172.5	
	AB	4,004,100	01/18/77	Takimoto	179	15 BS	
	AC	4,077,016	02/28/78	Sanders et al.	331	4	
	AD	4,096,402	06/20/78	Schroeder et al.	307	362	
	AE	4,404,474	09/13/83	Dingwall	307	260	
	AF	4,481,625	11/06/84	Roberts et al.	370	85	
	AG	4,508,983	04/02/85	Allgood et al.	307	577	
	AH	4,511,846	04/16/85	Nagy et al.	328	164	
	AI	4,514,647	04/30/85	Shoji	307	269	
	AJ	4,524,448	06/18/85	Hullwegen	375	118	
	AK	4,573,017	02/25/86	Levine	327	114	
	AL	4,600,895	07/15/86	Landsman	331	1 A	
	AM	4,603,320	07/29/86	Farago	341	89	
	AN	4,638,187	01/20/87	Boler et al.	307	451	
	AO	4,638,451	01/20/87	Hester et al.	395	889	
	AP	4,687,951	08/18/87	McElroy	307	269	
	AQ	4,727,541	02/23/88	Mori et al.	370	112	
	AR	4,746,996	05/24/88	Furuhata et al.	360	36.2	
	AS	4,773,085	09/20/88	Cordell	375	120	
	AT	4,789,796	12/06/88	Foss	307	443	
	AU	4,818,995	04/04/89	Takahashi et al.	341	94	
	AV	4,893,087	01/09/90	Davis	328	14	
	AW	4,902,986	02/20/90	Lesmeister	331	25	
	AX	4,953,128	08/28/90	Kawai et al.	365	194	
	AY	4,958,088	09/18/90	Farah-Bakhsh et al.	307	443	
	AZ	4,972,470	11/20/90	Farago	380	3	

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*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	BA	4,984,204	01/08/91	Sato et al.	365	189.11	
	BB	5,020,023	05/28/91	Smith	364	900	
	BC	5,038,115	08/06/91	Myers et al.	331	2	
	BD	5,062,082	10/29/91	Choi	365	230.06	
	BE	5,075,569	12/24/91	Branson	307	270	
	BF	5,086,500	02/04/92	Greub	395	550	
	BG	5,087,828	02/11/92	Sato et al.	307	269	
	BH	5,122,690	06/16/92	Bianchi	307	475	
	BI	5,128,560	07/07/92	Chern et al.	307	475	
	BJ	5,128,563	07/07/92	Hush et al.	307	482	
	BK	5,130,565	07/14/92	Girmay	307	265	
	BL	5,134,311	07/28/92	Biber et al.	307	270	
	BM	5,150,186	09/22/92	Pinney et al.	357	42	
	BN	5,165,046	11/17/92	Hesson	307	270	
	BO	5,168,199	12/01/92	Huffman et al.	315	370	
	BP	5,179,298	01/12/93	Hirano et al.	307	443	
	BQ	5,182,524	01/26/93	Hopkins	330	149	
	BR	5,194,765	03/16/93	Dunlop et al.	307	443	
	BS	5,212,601	05/18/93	Wilson	360	51	
	BT	5,220,208	06/15/93	Schenck	307	443	
	BU	5,223,755	06/29/93	Richley	307	603	
	BV	5,229,929	07/20/93	Shimizu et al.	363	98	
	BW	5,233,314	08/03/93	McDermott et al.	331	17	
	BX	5,233,564	08/03/93	Ohshima et al.	365	230.05	
	BY	5,239,206	08/24/93	Yanai	307	272.2	
	BZ	5,243,703	09/07/93	Farmwald et al.	395	325	

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*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	CA	5,254,883	10/19/93	Horowitz et al.	307	443	
	CB	5,256,989	10/26/93	Parker et al.	331	1 A	
	CC	5,257,294	10/26/93	Pinto et al.	375	120	
	CD	5,268,639	12/07/93	Gasbarro et al.	324	158 R	
	CE	5,272,729	12/21/93	Bechade et al.	375	118	
	CF	5,274,276	12/28/93	Casper et al.	307	443	
	CG	5,276,642	01/04/94	Lee	365	189.04	
	CH	5,278,460	01/11/94	Casper	307	296.5	
	CI	5,281,865	01/25/94	Yamashita et al.	307	279	
	CJ	5,283,631	02/01/94	Koerner et al.	307	451	
	CK	5,289,580	02/22/94	Latif et al.	395	275	
	CL	5,295,164	03/15/94	Yamamura	375	120	
	CM	5,304,952	04/19/94	Quiet et al.	331	1 A	
	CN	5,311,481	05/10/94	Casper et al.	365	230.06	
	CO	5,311,483	05/10/94	Takasugi	365	233	
	CP	5,313,431	05/17/94	Uruma et al.	365	230.05	
	CQ	5,315,388	05/24/94	Shen et al.	348	718	
	CR	5,321,368	06/14/94	Hoelzle	328	63	
	CS	5,337,285	08/09/94	Ware et al.	365	227	
	CT	5,341,405	08/23/94	Mallard, Jr.	375	120	
	CU	5,347,177	09/13/94	Lipp	307	443	
	CV	5,347,179	09/13/94	Casper et al.	307	451	
	CW	5,355,391	10/11/94	Horowitz et al.	375	36	
	CX	5,361,002	11/1/94	Casper	327	530	
	CY	5,367,649	11/22/94	Cedar	395	375	
	CZ	5,379,299	01/03/95	Schwartz	370	108	

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*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	DA	5,390,308	02/14/95	Ware et al.	395	400	
	DB	5,400,283	03/21/95	Raad	365	203	
	DC	5,402,389	03/28/95	Flannagan et al.	365	233	
	DD	5,408,640	04/18/95	MacIntyre et al.	395	550	
	DE	5,410,263	04/25/95	Waizman	327	141	
	DF	5,416,436	05/16/95	Rainard	327	270	
	DG	5,416,909	05/16/95	Long et al.	395	275	
	DH	5,420,544	05/30/95	Ishibashi	331	11	
	DI	5,428,311	06/27/95	McClure	327	276	
	DJ	5,428,317	06/27/95	Sanchez et al.	331	1 A	
	DK	5,430,408	07/04/95	Ovens et al.	327	407	
	DL	5,430,676	07/04/95	Ware et al.	365	189.02	
	DM	5,432,823	07/11/95	Gasbarro et al.	375	356	
	DN	5,438,545	08/01/95	Sim	365	189.05	
	DO	5,440,260	08/08/95	Hayashi et al.	327	278	
	DP	5,440,514	08/08/95	Flannagan et al.	365	194	
	DQ	5,444,667	08/22/95	Obara	365	233	
	DR	5,446,696	08/29/95	Ware et al.	365	222	
	DS	5,448,193	09/05/95	Baumert et al.	327	156	
	DT	5,451,898	09/19/95	Johnson	327	563	
	DU	5,457,407	10/10/95	Shu et al.	326	30	
	DV	5,465,076	11/07/95	Yamauchi et al.	331	179	
	DW	5,473,274	12/05/95	Reilly et al.	327	159	
	DX	5,473,575	12/05/95	Farmwald et al.	365	230.06	
	DY	5,473,639	12/05/95	Lee et al.	375	376	
	DZ	5,485,490	01/16/96	Leung et al.	375	371	

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*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	EA	5,488,321	01/30/96	Johnson	327	66	
	EB	5,489,864	02/06/96	Ashuri	327	161	
	EC	5,497,127	03/05/96	Sauer	331	17	
	ED	5,497,355	03/05/96	Mills et al.	365	230.08	
	EE	5,498,990	03/12/96	Leung et al.	327	323	
	EF	5,500,808	03/19/96	Wang	364	578	
	EG	5,502,672	03/26/96	Kwon	365	189.05	
	EH	5,506,814	04/09/96	Hush et al.	365	230.03	
	EI	5,508,638	04/16/96	Cowles et al.	326	38	
	EJ	5,513,327	04/30/96	Farmwald et al.	395	309	
	EK	5,532,714	07/02/96	Knapp et al.	345	114	
	EL	5,539,345	07/23/96	Hawkins	327	150	
	EM	5,544,124	08/06/96	Zagar et al.	365	230.08	
	EN	5,544,203	08/06/96	Casasanta et al.	375	376	
	EO	5,550,783	08/27/96	Stephens, Jr. et al.	365	233	
	EP	5,552,727	09/03/96	Nakao	327	159	
	EQ	5,555,429	09/17/96	Parkinson et al.	395	800	
	ER	5,557,224	09/17/96	Wright et al.	327	115	
	ES	5,557,781	09/17/96	Stones et al.	395	550	
	ET	5,563,546	10/08/96	Tsukada	327	408	
	EU	5,568,075	10/22/96	Curran et al.	327	172	
	EV	5,568,077	10/22/96	Sato et al.	327	199	
	EW	5,572,557	11/05/96	Aoki	375	376	
	EX	5,572,722	11/05/96	Vogley	395	555	
	EY	5,574,698	11/12/96	Raad	365	230.06	
	EZ	5,576,645	11/19/96	Farwell	327	94	

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*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	FA	5,577,236	11/19/96	Johnson et al.	395	551	
	FB	5,578,940	11/26/96	Dillon et al.	326	30	
	FC	5,578,941	11/26/96	Sher et al.	326	34	
	FD	5,579,326	11/26/96	McClure	371	61	
	FE	5,581,197	12/03/96	Motley et al.	326	30	
	FF	5,589,788	12/31/96	Goto	327	276	
	FG	5,590,073	12/31/96	Arakawa et al.	365	185.08	
	FH	5,594,690	01/14/97	Rothenberger et al.	365	189.01	
	FI	5,614,855	03/25/97	Lee et al.	327	158	
	FJ	5,619,473	04/08/97	Hotta	365	238.5	
	FK	5,621,340	04/15/97	Lee et al.	327	65	
	FL	5,621,690	04/15/97	Jungroth et al.	365	200	
	FM	5,621,739	04/15/97	Sine et al.	371	22.1	
	FN	5,627,780	05/06/97	Malhi	365	185.09	
	FO	5,627,791	05/06/97	Wright et al.	365	222	
	FP	5,631,872	05/20/97	Naritake et al.	365	227	
	FQ	5,636,163	06/03/97	Furutani et al.	365	233	
	FR	5,636,173	06/03/97	Schaefer	365	230.03	
	FS	5,636,174	06/03/97	Rao	365	230.03	
	FT	5,638,335	06/10/97	Akiyama et al.	365	230.03	
	FU	5,646,904	07/08/97	Ohno et al.	365	233	
	FV	5,652,530	07/29/97	Ashuri	326	93	
	FW	5,657,289	08/12/97	Hush et al.	365	230.05	
	FX	5,657,481	08/12/97	Farmwald et al.	395	551	
	FY	5,663,921	09/02/97	Pascucci et al.	365	233	
	FZ	5,666,322	09/09/97	Conkle	365	233	

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	GA	5,668,763	09/16/97	Fujioka et al.	365	200	
	GB	5,668,774	09/16/97	Furatani	365	233	
	GC	5,673,005	09/30/97	Pricer	331	1 R	
	GD	5,675,274	10/07/97	Kobayashi et al.	327	158	
	GE	5,675,588	10/07/97	Maruyama et al.	371	20.4	
	GF	5,692,165	11/25/97	Jeddeloh et al.	395	551	
	GG	5,694,065	12/02/97	Hamasaki et al.	327	108	
	GH	5,708,611	01/13/98	Iwamoto	365	233 X	
	GI	5,712,580	01/27/98	Baumgartner et al.	327	12	
	GJ	5,719,508	02/17/98	Daly	327	12	
	GK	5,737,342	04/07/98	Ziporovich	371	25.1	
	GL	5,740,123	04/14/98	Uchida	365	233	
	GM	5,751,665	05/12/98	Tanoi	368	120	
	GN	5,767,715	06/16/98	Marquis et al.	327	159	
	GO	5,768,177	06/16/98	Sakuragi	365	194	
	GP	5,774,699	06/30/98	Nagae	395	551	
	GQ	5,778,214	07/07/98	Taya et al.	395	551	
	GR	5,781,499	07/14/98	Koshikawa	365	233	
	GS	5,784,422	07/21/98	Heermann	375	355	
	GT	5,789,947	08/04/98	Sato	327	3	
	GU	5,790,612	08/04/98	Chengson et al.	375	373	
	GV	5,794,020	08/11/98	Tanaka et al.	395	552	
	GW	5,805,931	09/08/98	Morzano et al.	395	884	
	GX	5,812,619	09/22/98	Runaldue	375	376	
	GY	5,822,314	10/13/98	Chater-Lea	370	337	
	GZ	5,831,929	11/03/98	Manning	365	233	

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	HA	5,841,707	11/24/98	Cline et al.	365	194	
	HB	5,852,378	12/22/98	Keeth	327	171	
	HC	5,872,959	02/16/99	Nguyen et al.	395	552	
	HD	5,889,829	03/30/99	Chiao et al.	375	376	
	HE	5,898,242	04/27/99	Peterson	327	278	
	HF	5,898,674	04/27/99	Mawhinney et al.	370	247	
	HG	5,917,760	06/29/99	Millar	365	194	
	HH	5,920,518	07/06/99	Harrison et al.	365	233	
	HI	5,926,047	07/20/99	Harrison	327	159	
	HJ	5,926,436	07/20/99	Toda et al.	365	236	
	HK	5,940,608	08/17/99	Manning	395	551	
	HL	5,940,609	08/17/99	Harrison	395	559	
	HM	5,946,244	08/31/99	Manning	365	194	
	HN	5,953,284	09/14/99	Baker et al.	365	233	
	HO	5,964,884	10/12/99	Partovi et al.	713	503	
	HP	5,990,719	11/23/99	Dai et al.	327	244	
	HQ	6,005,823	12/21/99	Martin et al.	365	230.08	
	HR	6,011,732	01/04/00	Harrison et al.	365	194	
	HS	6,016,282	01/18/00	Keeth	365	233	
	HT	6,023,489	02/08/00	Hatch	375	208	
	HU	6,026,050	02/15/00	Baker et al.	635	233	
	HV	6,029,250	02/22/00	Keeth	713	400	
	HW	6,038,219	03/14/00	Mawhinney et al.	370	242	
	HX	6,067,592	05/23/00	Farmwald et al.	710	104	
	HY	6,101,152	08/08/00	Farmwald et al.	365	233	
	HZ	6,101,197	08/08/00	Keeth et al.	370	517	

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FORM PTO-1449  
(REV.7-80)U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.  
500444.04APPLICATION NO.  
Not Yet Assigned**INFORMATION DISCLOSURE STATEMENT***(Use several sheets if necessary)*

APPLICANTS

Troy A. Manning

FILING DATE

Concurrently herewith

GROUP ART UNIT

Not Yet Assigned

**U.S. PATENT DOCUMENTS**

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	IA	6,105,157	08/15/00	Miller	714	744	
	IB	6,147,905	11/14/00	Seino	365	185.11	
	IC	6,147,916	11/14/00	Ogura	365	203	
	ID	6,160,423	12/12/00	Haq	327	41	
	IE	6,262,921 B1	07/17/01	Manning	365	194	
	IF	6,269,451 B1	07/31/01	Mullarkey	713	401	
	IG	6,298,450 B1	10/02/01	Liu et al.	713	502	
	IH	6,327,196 B1	12/04/01	Mullarkey	365	194	
	II	6,338,127 B1	01/08/02	Manning	711	167	
	IJ	6,378,079 B1	04/23/02	Mullarkey	713	401	
	IK	6,499,111 B2	12/24/02	Mullarkey	713	401	

**FOREIGN PATENT DOCUMENTS**

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	IL	0 171 720 A2	02/19/86	EP			X	
	IM	6-1237512	10/22/86	JP (Abstract Only)			X	
	IN	0 295 515 A1	12/21/88	EP			X	
	IO	2-112317	4/25/90	JP (+ Abstract)			X	
	IP	0 406 786 A1	1/9/91	EP			X	
	IQ	0 450 871 A2	10/9/91	EP			X	
	IR	0 476 585 A3	3/25/92	EP			X	
	IS	4-135311	5/8/92	JP (+ Abstract)			X	
	IT	5-136664	6/1/93	JP (+ Abstract)			X	
	IU	5-282868	10/29/93	JP (Abstract Only)			X	
	IV	WO 94/29871	12/22/94	PCT			X	

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FOREIGN PATENT DOCUMENTS								
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	IW	0 655 741 A2	5/31/95	EP			X	
	IX	0 655 834 A1	5/31/95	EP			X	
	IY	WO 95/22200	8/17/95	PCT			X	
	IZ	WO 95/22206	8/17/95	PCT			X	
	JA	0 680 049 A2	11/2/95	EP			X	
	JB	0-7319577	12/8/95	JP (+ Abstract)			X	
	JC	0 703 663 A1	3/27/96	EP			X	
	JD	0 704 848 A3	4/3/96	EP			X	
	JE	0 704 975 A1	4/3/96	EP			X	
	JF	WO 96/10866	4/11/96	PCT			X	
	JG	0 767 538 A1	4/9/97	EP			X	
	JH	WO 97/14289	4/24/97	PCT			X	
	JI	WO 97/42557	11/13/97	PCT			X	
OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
	JJ	Alvarez, J. et al. "A Wide-Bandwidth Low Voltage PLL for PowerPC <sup>TM</sup> Microprocessors" IEEE IEICE Trans. Electron., Vol. E-78. No. 6, June 1995, pp. 631-639						
	JK	Anonymous, "400MHz SDRAM, 4M X 16 SDRAM Pipelined, Eight Bank, 2.5 V Operation," SDRAM Consortium Advance Sheet, published throughout the United States, pp.1-22						
	JL	Anonymous, "Draft Standard for a High-Speed Memory Interface (SyncLink)", Microprocessor and Microcomputer Standards Subcommittee of the IEEE Computer Society, Copyright 1996 by the Institute of Electrical and Electronics Engineers, Inc., New York, NY, pp. 1-56						
	JM	Anonymous, "Programmable Pulse Generator", IBM Technical Disclosure Bulletin, Vol. 17, No. 12, May 1975, pp. 3553-3554						
	JN	Arai, Y. et al., "A Time Digitizer CMOS Gate-Array with a 250 ps Time Resolution", XP 000597207, IEEE Journal of Solid-State Circuits, Vol. 31, No.2, February 1996, pp. 212-220						
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**OTHER PRIOR ART** (Including Author, Title, Date, Pertinent Pages, Etc.)

	JO	Anonymous, "Pulse Combining Network", IBM Technical Disclosure Bulletin, Vol. 32, No. 12, May 1990, pp. 149-151
	JP	Anonymous, "Variable Delay Digital Circuit", IBM Technical Disclosure Bulletin, Vol. 35, No. 4A, September 1992, pp. 365-366
	JQ	Arai, Y. et al., "A CMOS Four Channel x 1K Time Memory LSI with 1-ns/b Resolution", IEEE Journal of Solid-State Circuits, Vol. 27, No. 3, M, 8107 March, 1992, No. 3, New York, US, pp. 359-364 and pp. 528-531
	JR	Aviram, A. et al., "OBTAINING HIGH SPEED PRINTING ON THERMAL SENSITIVE SPECIAL PAPER WITH A RESISTIVE RIBBON PRINT HEAD", IBM Technical Disclosure Bulletin, Vol. 27, No. 5, October 1984, pp. 3059-3060
	JS	Bazes, M., "Two Novel Fully Complementary Self-Biased CMOS Differential Amplifiers", IEEE Journal of Solid-State Circuits, Vol. 26, No. 2, February 1991, pp. 165-168
	JT	Chapman, J. et al., "A Low-Cost High-Performance CMOS Timing Vernier for ATE", IEEE International Test Conference, Paper 21.2, 1995, pp. 459-468
	JU	Cho, J. "Digitally-Controlled PLL with Pulse Width Detection Mechanism for Error Correction", ISSCC 1997, Paper No. SA 20.3, pp. 334-335
	JV	Christiansen, J., "An Integrated High Resolution CMOS Timing Generator Based on an Array of Delay Locked Loops", IEEE Journal of Solid-State Circuits, Vol. 31, No. 7, July 1996, pp. 952-957
	JW	Combes, M. et al., "A Portable Clock Multiplier Generator Using Digital CMOS Standard Cells", IEEE Journal of Solid-State Circuits, Vol. 31, No. 7, July 1996, pp. 958-965
	JX	Donnelly, K. et al., "A 660 MB/s Interface Megacell Portable Circuit in 0.3 $\mu$ m-0.7 $\mu$ m CMOS ASIC", IEEE Journal of Solid-State Circuits, Vol. 31, No. 12, December 1996, pp. 1995-2001
	JY	Goto, J. et al., "A PLL-Based Programmable Clock Generator with 50- to 350-MHz Oscillating Range for Video Signal Processors", IEICE Trans. Electron., Vol. E77-C, No. 12, December 1994, pp. 1951-1956
	JZ	Gustavson, David B., et al., "IEEE Standard for Scalable Coherent Interface (SCI)," IEEE Computer Society, IEEE Std. 1596-1992, August 2, 1993.
	KA	Hamamoto, T., "400-MHz Random Column Operating SDRAM Techniques with Self-Skew Compensation", IEEE Journal of Solid-State Circuits, Vol. 33, No. 5, May 1998, pp. 770-778
	KB	Ishibashi, A. et al., "High-Speed Clock Distribution Architecture Employing PLL for 0.6 $\mu$ m CMOS SOG", IEEE Custom Integrated Circuits Conference, 1992, pp. 27.6.1-27.6.4

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<b>OTHER PRIOR ART</b> (Including Author, Title, Date, Pertinent Pages, Etc.)	
KC	Kim, B. et al., "A 30MHz High-Speed Analog/Digital PLL in 2 $\mu$ m CMOS", ISSCC, February 1990
KD	Kikuchi, S. et al., "A GATE-ARRAY-BASED 666MHz VLSI TEST SYSTEM", IEEE International Test Conference, Paper 21.1, 1995, pp. 451-458
KE	Ko, U. et al., "A 30-ps JITTER, 3.6- $\mu$ s LOCKING, 3.3-VOLT DIGITAL PLL FOR CMOS GATE ARRAYS", IEEE Custom Integrated Circuits Conference, 1993, pp. 23.3.1-23.3.4
KF	Lee, T. et al., "A 2.5V Delay-Locked Loop for an 18Mb 500MB/s DRAM", IEEE International Solid-State Circuits Conference Digest of Technical Papers, Paper No. FA 18.6, 1994, pp. 300-301
KG	Lesmeister, G., "A DENSELY INTEGRATED HIGH PERFORMANCE CMOS TESTER", International Test Conference, Paper 16.2, 1991, pp. 426-429
KH	Ljuslin, C. et al., "An Integrated 16-channel CMOS Time to Digital Converter", IEEE Nuclear Science Symposium & Medical Imaging Conference Record, Vol. 1, 1993, pp. 625-629
KI	Maneatis, J., "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1723-1732
KJ	Nakamura, M. et al., "A 156 Mbps CMOS Clock Recovery Circuit for Burst-mode Transmission", Symposium on VLSI Circuits Digest of Technical Papers, 1996, pp. 122-123
KK	Nielson, E., "Inverting latches make simple VCO", EDN, June 19, 1997
KL	Novof, I. et al., "Fully Integrated CMOS Phase-Locked Loop with 15 to 240 MHz Locking Range and $\pm 50$ ps Jitter", IEEE Journal of Solid-State Circuits, Vol. 30, No. 11, November 1995, pp. 1259-1266
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KN	Santos, D. et al., "A CMOS Delay Locked Loop And Sub-Nanosecond Time-to-Digital Converter Chip", IEEE Nuclear Science Symposium and Medical Imaging Conference Record, Vol. 1, October 1995, pp. 289-291
KO	Shirotori, T. et al., "PLL-based, Impedance Controlled Output Buffer", 1991 Symposium on VLSI Circuits Digest of Technical Papers, pp. 49-50.
KP	Sidiropoulos, S. et al., "A 700-Mb/s/pin CMOS Signaling Interface Using Current Integrating Receivers", IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, May 1997, pp. 681-690.
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	KQ	Sidiropoulos, S. et al., "A CMOS 500 Mbps/pin synchronous point to point link interface", IEEE Symposium on VLSI Circuits Digest of Technical Papers, 1994, pp. 43-44
	KR	Sidiropoulos, S. et al., "A Semi-Digital DLL with Unlimited Phase Shift Capability and 0.08-400MHz Operating Range," IEEE International Solid State Circuits Conference, February 8, 1997, pp.332-333
	KS	Soyuer, M. et al., "A Fully Monolithic 1.25GHz CMOS Frequency Synthesizer", IEEE Symposium on VLSI Circuits Digest of Technical Papers, 1994, pp. 127-128
	KT	Taguchi, M. et al., "A 40-ns 64-Mb DRAM with 64-b Parallel Data Bus Architecture", IEEE Journal of Solid-State Circuits, Vol. 26, No. 11, November 1991, pp. 1493-1497
	KU	Tanoi, S. et al., "A 250-622 MHz Deskew and Jitter-Suppressed Clock Buffer Using a Frequency- and Delay-Locked Two-Loop Architecture", 1995 Symposium on VLSI Circuits Digest of Technical Papers, Vol. 11, No. 2, pp. 85-86
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	KW	von Kaenel, V. et al., "A 320 MHz, 1.5 mW @ 1.35 V CMOS PLL for Microprocessor Clock Generation", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1715-1722
	KX	Watson, R. et al., "Clock Buffer Chip with Absolute Delay Regulation Over Process and Environmental Variations", IEEE Custom Integrated Circuits Conference, 1992, pp. 25.2.1-25.2.5
	KY	Yoshimura, T. et al. "A 622-Mb/s Bit/Frame Synchronizer for High-Speed Backplane Data Communication", IEEE Journal of Solid-State Circuits, Vol. 31, No. 7, July 1996, pp. 1063-1066

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